| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|---|---|---|---|---|---|
| 1 | BRS | L1 | 828684 | processor microprocessor mpu cpu | US-PGPUB; USPAT | 2006/09/20 13:02 |
| 2 | BRS | L2 | 185063 | (reduc$3 conserv$3 manage$4) near3 power | US-PGPUB; USPAT | 2006/09/20 13:04 |
| 3 | BRS | L3 | 72111 | 1 and 2 | US-PGPUB; USPAT | 2006/09/20 13:04 |
| 4 | BRS | L4 | 139 | dynamic adj power adj management | US-PGPUB; USPAT | 2006/09/20 13:04 |
| 5 | BRS | L5 | 133 | 3 and 4 | US-PGPUB; USPAT | 2006/09/20 13:06 |
| 6 | BRS | L6 | 3454 | (machine adj state adj register) or msr | US-PGPUB; USPAT | 2006/09/20 13:07 |
| 7 | BRS | L7 | 4 | 5 and 6 | US-PGPUB; USPAT | 2006/09/20 13:38 |
| 8 | BRS | L8 | 6242 | state adj register | US-PGPUB; USPAT | 2006/09/20 13:39 |
| 9 | BRS | L9 | 21826 | control adj register | US-PGPUB; USPAT | 2006/09/20 13:41 |
| 10 | BRS | L10 | 0 | lagacy near5 width | US-PGPUB; USPAT | 2006/09/20 13:45 |
| 11 | BRS | L11 | 31 | legacy near5 width | US-PGPUB; USPAT | 2006/09/20 13:45 |
| 12 | BRS | L12 | 11 | 2 and 11 | US-PGPUB; USPAT | 2006/09/20 13:52 |
| 13 | BRS | L13 | 20 | 11 not 12 | US-PGPUB; USPAT | 2006/09/20 14:02 |
| 14 | BRS | L14 | 0 | 11 same (instruction register) | US-PGPUB; USPAT | 2006/09/20 14:03 |
| 15 | BRS | L15 | 26317 | 8 or 9 | US-PGPUB; USPAT | 2006/09/20 14:03 |
| 16 | BRS | L16 | 7979 | ("64" adj bit$1) with ("32" adj bit$1) | US-PGPUB; USPAT | 2006/09/20 14:04 |
| 17 | BRS | L17 | 1895 | 15 and 16 | US-PGPUB; USPAT | 2006/09/20 14:05 |
| 18 | BRS | L18 | 34526 | register near3 (portion$1 block$1 partition$3) | US-PGPUB; USPAT | 2006/09/20 14:06 |
| 19 | BRS | L19 | 1326 | 18 same upper same lower | US-PGPUB; USPAT | 2006/09/20 14:10 |
| 20 | BRS | L20 | 98 | 17 and 19 | US-PGPUB; USPAT | 2006/09/20 14:10 |
| 21 | BRS | L21 | 98 | 1 and 20 | US-PGPUB; USPAT | 2006/09/20 14:11 |
| 22 | BRS | L22 | 72 | 2 and 20 | US-PGPUB; USPAT | 2006/09/20 14:12 |
| 23 | BRS | L23 | 82724 | clock same voltage | US-PGPUB; USPAT | 2006/09/20 14:13 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|---|---|---|---|---|---|
| 24 | BRS | L24 | 71 | 22 and 23 | US-PGPUB; USPAT | 2006/09/20 14:13 |
| 25 | BRS | L25 | 3315 | 713/300.ccls. 713/320.ccls. | US-PGPUB; USPAT | 2006/09/20 14:14 |
| 26 | BRS | L26 | 1916 | 713/322-324.ccls. | US-PGPUB; USPAT | 2006/09/20 14:14 |
| 27 | BRS | L27 | 4550 | 25 or 26 | US-PGPUB; USPAT | 2006/09/20 14:17 |
| 28 | BRS | L28 | 1 | 24 and 27 | US-PGPUB; USPAT | 2006/09/20 14:20 |
| 29 | BRS | L29 | 4 | (architected adj bits) near5 register | US-PGPUB; USPAT | 2006/09/20 14:29 |
| 30 | BRS | L30 | 3631 | ((state status) adj bit$1) near5 register | US-PGPUB; USPAT | 2006/09/20 14:30 |
| 31 | BRS | L31 | 70 | 24 and 30 | US-PGPUB; USPAT | 2006/09/20 14:30 |
| 32 | BRS | L32 | 32136 | idle near5 (status state mode) | US-PGPUB; USPAT | 2006/09/20 14:31 |
| 33 | BRS | L33 | 70 | 31 and 32 | US-PGPUB; USPAT | 2006/09/20 14:35 |
| 34 | BRS | L34 | 1 | 24 not 33 | US-PGPUB; USPAT | 2006/09/20 14:37 |
| 35 | BRS | L35 | 39265 | datapath or (data adj path) | US-PGPUB; USPAT | 2006/09/20 14:38 |
| 36 | BRS | L36 | 478029 | (size width) near5 (chang$3 alter$3 reduc$3) | US-PGPUB; USPAT | 2006/09/20 14:38 |
| 37 | BRS | L37 | 475 | 35 same 36 | US-PGPUB; USPAT | 2006/09/20 14:39 |
| 38 | BRS | L38 | 109 | 3 and 37 | US-PGPUB; USPAT | 2006/09/20 14:40 |
| 39 | BRS | L39 | 105 | 38 and (register alu fpu) | US-PGPUB; USPAT | 2006/09/20 14:41 |
| 40 | BRS | L40 | 105 | 39 not 33 | US-PGPUB; USPAT | 2006/09/20 14:41 |
| 41 | BRS | L41 | 39 | 23 and 40 | US-PGPUB; USPAT | 2006/09/20 15:21 |
| 42 | BRS | L42 | 5 | 27 and 38 | US-PGPUB; USPAT | 2006/09/20 15:23 |
| 43 | BRS | L43 | 5 | "645024".ap. | US-PGPUB; USPAT | 2006/09/20 15:23 |
| 44 | BRS | L44 | 1 | 43 and (media medium) | US-PGPUB; USPAT | 2006/09/20 15:24 |
| 45 | BRS | L45 | 1 | 44 and (wave signal) | US-PGPUB; USPAT | 2006/09/20 15:24 |

| | Type | L # | Hits | Search Text | DBs | Time Stamp |
|---|---|---|---|---|---|---|
| 1 | BRS | L1 | 8371 | register same control$4 same voltage same (clock frequency) | US-PGPUB; USPAT | 2006/09/20 20:05 |
| 2 | BRS | L2 | 1543 | register with control$4 with voltage with (clock frequency) | US-PGPUB; USPAT | 2006/09/20 20:07 |
| 3 | BRS | L3 | 828684 | processor microprocessor cpu mpu | US-PGPUB; USPAT | 2006/09/20 20:07 |
| 4 | BRS | L4 | 739 | 2 and 3 | US-PGPUB; USPAT | 2006/09/20 20:08 |
| 5 | BRS | L5 | 185063 | (reduc$3 conserv$3 manage$4) near3 power | US-PGPUB; USPAT | 2006/09/20 20:08 |
| 6 | BRS | L6 | 250 | 4 and 5 | US-PGPUB; USPAT | 2006/09/20 20:09 |
| 7 | BRS | L7 | 94914 | register near5 (bit position) | US-PGPUB; USPAT | 2006/09/20 20:10 |
| 8 | BRS | L8 | 90 | 6 and 7 | US-PGPUB; USPAT | 2006/09/20 20:10 |